layer P, the original leg is split into three legs cleanly isolated by the resultant voided (i.e., subtracted) extend area SE'. The result of all of the foregoing is that candidate transistors are re-legged in such a way that gate, source and drain connectivity are maintained.--.

REMARKS

This Preliminary Amendment is being filed prior to examination on the merits in the above-identified application.

Pending Claims

At entry of this paper, Claims 1-16 are pending for consideration in the present application. No claims have been cancelled, added or amended.

Amendments to the Specification

Amendments have been made in the specification to correct minor typographical errors and omissions. No new matter has been added. Attached hereto is "Appendix A-Marked Version" showing the amendments to the specification with underlining and brackets to indicate additions and deletions, respectively.

Examiner Invited To Telephone

The Examiner is herein invited to telephone the undersigned attorneys at the local Washington, D.C. area telephone number of 703/312-6600 for discussing any Examiner's Amendments or other suggested actions for accelerating prosecution and moving the present application to allowance.

Conclusion

In view of the foregoing amendments and remarks, Applicant respectfully submits that the claims listed above as presently being under consideration in the application are now in condition for allowance. Accordingly, early allowance of such claims is respectfully requested.

No Petition for extension or additional fees are required by the filing of this Preliminary Amendment. To whatever other extent is actually necessary, Applicant petitions for an extension of time §1.136. Please charge any shortage in fees due in connection with the filing of this paper to ATS&K Deposit Account No. 01-2135 (referencing Case No. 219.39069X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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Enclosures:
Appendix A-Marked Version

APPENDIX A-MARKED VERSION

IN THE SPECIFICATION:

Paragraph spanning pages 5 and 6:

FIG. 1 illustrates an example migration arrangement 100 (including an example compactor) in simplistic form, such FIG. being useful in explanation and understanding both background and example embodiments of the present invention. More specifically, shown is a source layout 110 fed to a compactor 120. The source layout 110 can be of any type of suitable code, for example, a non-exhaustive listing including Verilog or VHDL code. The compactor 120 further takes into consideration target process design rules 130 as well as user-specified constraints 140, and migrates the source layout 110 to a migrated layout 150 which is more compact and which complies with the inputted rules and constraints.

Single Full Paragraph on page 19:

The gate-expansion sub-arrangement implements gate expansion operations with respect to the FIG. 15 gate expansion treatment block 1510. As non-exhaustive examples, gate expansion candidates and/or gate expansion size may be automatically determined taking into consideration: the old design rules used to design the original source layout; the user-specified constraints 140 (as indicated by the FIG. 2 dashed arrow 290); the target process design rules 130 being used to design (i.e., compact) the layout (as indicated by the FIG. 2 dashed arrow 280); or, any combination thereof. The automatic re-legging arrangement 260 may also, or alternatively, allow a user to stipulate gate expansion candidates and/or gate expansion size. As further example embodiments, gate expansion may be globally

applied for all transistor re-legging candidates, or only selectively applied for a lesser number of the transistor re-legging candidates. As a final note, care must be taken with gate expansion so as not to overlap neighboring layout structures so as to maintain proper electrical isolation (i.e., avoid short-circuiting in the final migrated layout). With the foregoing in mind, FIG. 9 illustrates a gate-expanded layout where all three of the transistor re-legging candidates have expanded gate areas, i.e., T_{VE}, T_{YE}, T_{ZE}, whereas the other transistor areas T_W, T_X do not. Note the difference in the size of the gates aimed at re-legging and those that are not.

Paragraph spanning pages 24-26:

Discussion turns next to trimming of poly under the slots and also contact preparations. More particularly, once slots are defined by the above procedures, they are mathematically or arithmetically subtracted from the poly-silicon layer. Thus, an original normal leg is turned into a plurality of (e.g., three) thin legs connected in parallel. Trimming the poly-silicon leaves two uncovered diffusions between adjacent legs which is in the source node (and drain node) of two legs connected together. Assume that the source node is left as uncovered diffusion. It then must be connected to the right side of the original leg. In a similar way, the right uncovered diffusion, which is now the drain node, must be connected to the left side of the original leg. In order to ease this task, seeds of contacts covered by metal pads are implanted in the uncovered diffusion area. FIG. 12 shows an enlarged view with respect to trimming and contact placement/sizing of the FIG. 10 slots T_{YS1}, T_{YS2}. Of particular interest, note that while the two FIG. 12 slots have been illustrated unequally trimmed [unequally] in length, i.e., a FIG. 12 left-hand contact C is shorter

in length that a right-hand contact. A reason for this (similar to the reason as in FIG. 4) is to avoid potential electrical interference (e.g., short-circuiting) between the re-legging [contacts] contact seeds and a closely neighboring layout structure [structure] LS (e.g., a metal M1 edge). FIG. 13 illustrates a non-enlarged re-legged layout 1300 where trimming has been completed and a pair of contacts has been placed with respect to each of the aforementioned three transistor re-legging candidates. Finally, FIG. 14 show an enlarged view of only an upper portion of the FIG. 10 slots T_{ZS1}, T_{ZS2}, for the purpose of showing that, upon subtraction of the slot's extend area SE from the poly-silicon layer P, the original leg is split into three legs cleanly isolated by the resultant voided (i.e., subtracted) extend area SE'. The result of all of the foregoing is that candidate transistors are re-legged in such a way that gate, source and drain connectivity are maintained.